CSE369 Practice Problems (lec 4)

Unsigned Binary Representation

Convert the following 8-bit binary numbers into unsigned decimal:

1.1] `0 1 1 0 1 0 1 1`

1+2+8+32+64 = 107

1.2] `1 0 0 0 0 0 1 1`

1+2+128 = 131

1.3] `0 0 0 0 1 0 0 0`

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Signed Binary Representation

Convert the following 8-bit binary numbers into *signed* decimal assuming two's complement encoding:

2.1] `1 1 1 0 0 0 1 1`

1+2+32+64+(-128) = -29

2.2] `0 0 0 0 0 1 1 1`

1+2+4 = 7

2.3] `1 1 0 1 0 1 0 0`

4+16+64+(-128) = -44

Arithmetic and Overflow

Add the following four-bit numbers together. Complete their unsigned and signed representations. Report whether there was signed overflow and unsigned overflow.

3.1]

Binary

```
  0 0 0 1 1
+ 1 0 1 0 0
  1 0 1 1 1
```

Signed: -9

Unsigned: 23

Overflow?
[ ] yes
[x] no

Overflow?
[ ] yes
[x] no

3.2]

Binary

```
  1 1 1
  1 1 1 0 0
+ 0 0 1 0 0
  0 0 0 0 0
```

Signed: 0

Unsigned: 0

Overflow?
[ ] yes
[x] no

Overflow?
[x] yes
[ ] no

3.3]

(as -4+4 is 0)

Binary

```
  1       1
  1 0 0 0 1
+ 1 0 0 0 1
  0 0 0 1 0
```

Signed: 2

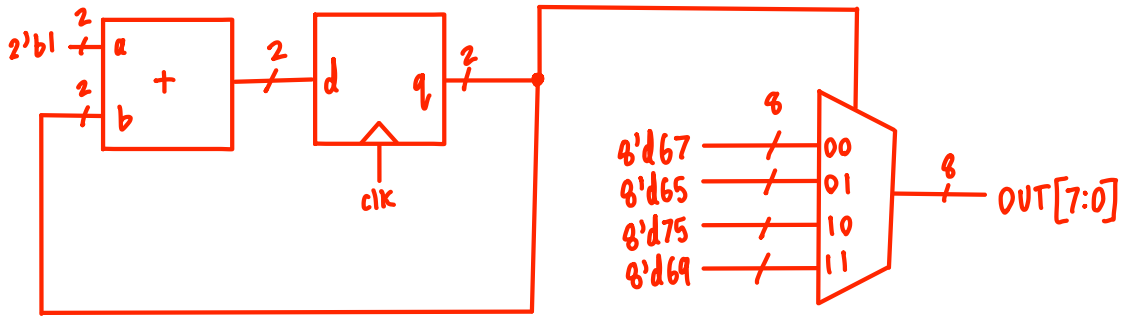
Unsigned: 2

Overflow?
[x] yes
[ ] no

Overflow?
[x] yes
[ ] no

Sequential Design

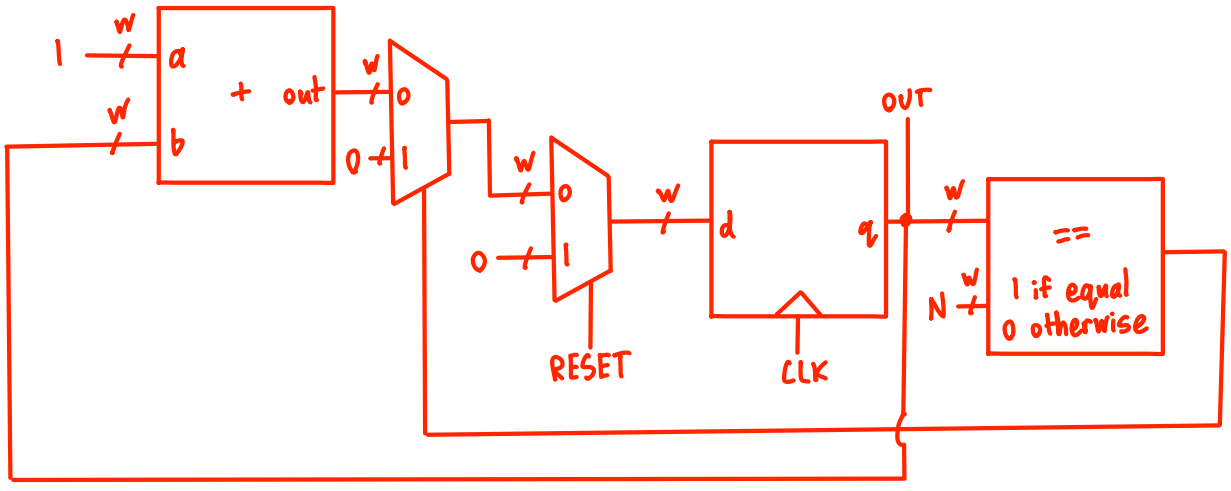
4.1] Draw a block diagram for a circuit that cycles through outputting the following four 8-bit numbers over and over again: 67, 65, 75, 69



4.2] Draw a block diagram for a circuit that counts up from 0 to parameter N

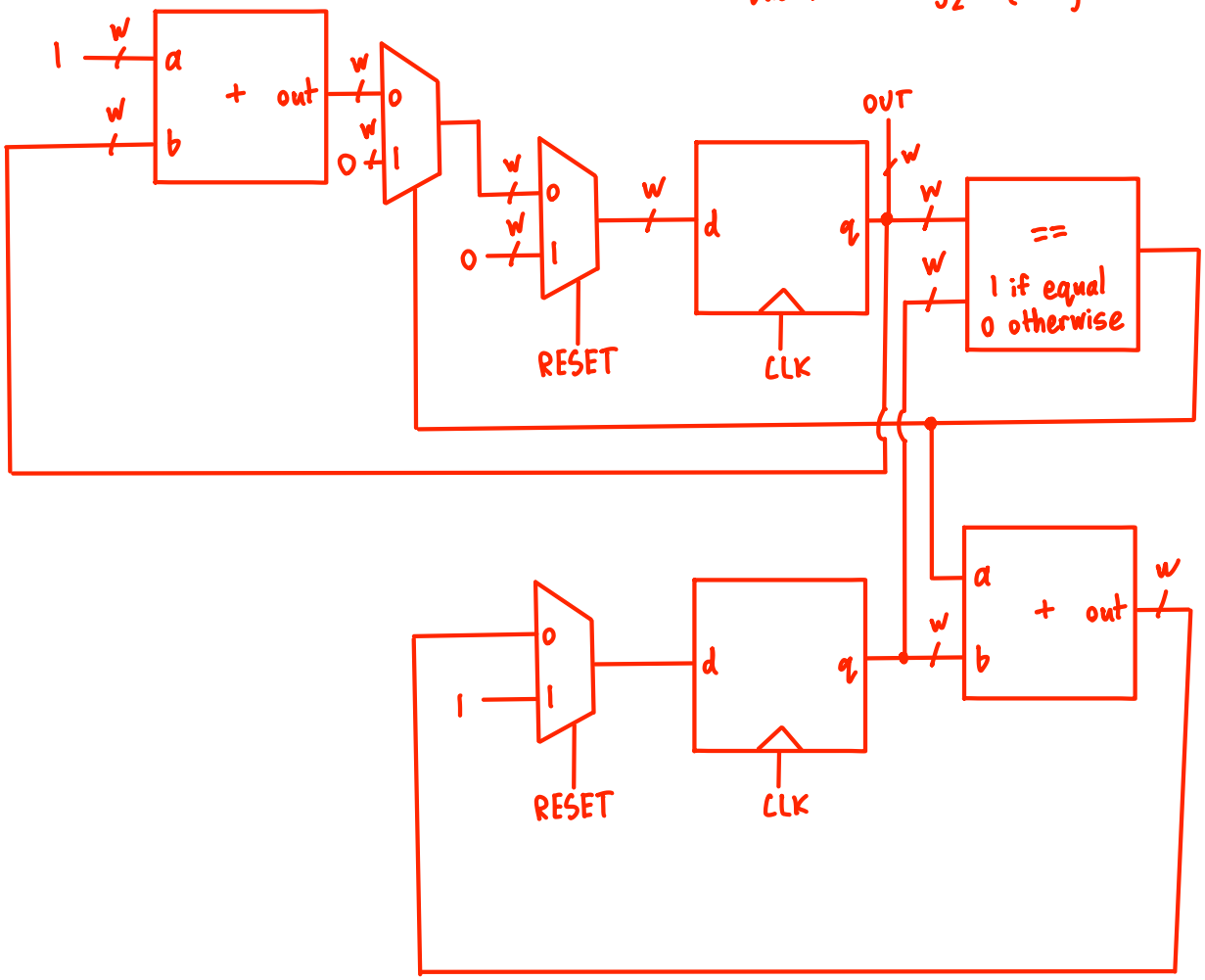
Hint: This will look very similar to the "perpetual timer" example from class, but it'll need another mux and a block to compare if two numbers are equal. You can treat this comparator as a "black box" whose implementation we take for granted (but you know enough to design that too, if you wanted to 😉)

bus widths = $\log_2 N$ (using "w" as shorthand)



4.3] Design a circuit that counts up from 0 to N and then starts over again, with N starting at 1 and increasing every time the sequence repeats. (eg: 0, 1, 0, 1, 2, 0, 1, 2, 3, 0, 1, 2, 3, 4, 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5, 6, 0, 1, 2, 3, 4, 5, 6, 7...)

bus widths = $\log_2 N$ (using "w" as shorthand)



4.4] Complete this timing diagram to show how the labelled signals in the circuit below change after reset. Assume no propagation delay.

